DERWENT-ACC-NO: 1986-306477

DERWENT-WEEK: 198647

TITLE: Digital demodulator clock generator with VCO - has phase control signals derived from window pulses and frequency control signals derived by comparing clock pulse intervals with limits

PATENT-ASSIGNEE: VICTOR CO OF JAPAN[VICO]

PRIORITY-DATA: 1985JP-0099900 (May 11, 1985) , 1984JP-0062849 (March 30, 1984)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
DE 3615952 A	November 13, 1986	N/A	035	N/A
DE 3615952 C	February 2, 1989	N/A	000	N/A
JP 61258534 A	November 15, 1986	N/A	000	N/A
US 4672329 A	June 9, 1987	N/A	000	N/A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
DE 3615952A	N/A	1986DE-3615952	May 12, 1986

JP 61258534A N/A
1985JP-0099900 May 11, 1985
US 4672329A N/A
1986US-0861437 May 9, 1986

INT-CL (IPC): H03L007/00, H03M005/12 , H04L007/00 , H04L025/40

ABSTRACTED-PUB-NO: DE 3615952A

BASIC-ABSTRACT:

The incoming bit stream produces window pulses in response to predetermined transitions between binary 1 and 0 in the bit stream for comparison with the clock pulses to produce in turn the phase control signal.

In a parallel frequency comparison circuit, two counts of clock pulses over long and short time intervals are fed to a comparator which determines the extent to which these counts fall outside low and high limits and to generate variable amplitude frequency control signals as a result. The frequency and phase control signals are combined in a mixer and used to control the VCO. The first count signals are switched out if the bit-stream frequency exceeds normal frequency.

ADVANTAGE - Overcomes instability resulting from speed variations in digital tape apperatus.

ABSTRACTED-PUB-NO: DE 3615952C

EQUIVALENT-ABSTRACTS:

The clock signal recovery circuit, for digital signals, uses a window pulse generator providing the window pulses in response to a given digital signal flank, fed to a phase comparator, for comparison with the recovered clock signals. The clock signals are recorded by a frequency discriminator counter during a time period defined by a reference frequency generator and the obtained count is compared with a given range to provide a frequency control signal. The output signals of the phase comparator and the frequency discriminator are fed to a mixer to provide a signal for a voltage-controlled oscillator providing the clock signal.

Similarly a second counter within the frequency discriminator records the clock signal over a second reference frequency generator period, to provide a second frequency control signal which is also supplied to the mixer.

USE - For digital receiver with rapid search facility. (15pp)

US 4672329A

A frequency comparator counts a clock pulse at long periodic intervals to

generate a count representing a long-term measurement of the instantaneous clock frequency and further counts it at shorter periodic intervals to generate a second count representing a short-term measurement of the instantaneous clock frequency. The first count is compared with the limits of a narrow range to generate a frequency control signal and the second count is compared with the limits of a wider range to produce a second frequency control signal.

When the clock frequency goes out of the wide range, the short-term clock frequency detection causes the second frequency control signal to be generated quickly at a point in time earlier than the time the first signal is generated.

ADVANTAGE - Clock frequency is pulled into wide range quickly for subsequent pull-in action into narrow range. (16pp)a

CHOSEN-DRAWING: Dwg.0/6

DERWENT-CLASS: W01

EPI-CODES: W01-A07; W01-A08A;